Sub B1

1. A method for forming a patterned microelectronics layer comprising:

providing a substrate having a contact region formed therein;

forming over the substrate a first lower sub-layer and a second upper sub-layer to provide a composite etch stop layer;

forming over the composite etch stop layer an inter-level metal dielectric (IMD) layer;

forming over the IMD layer a photoresist mask layer pattern of an interconnection line trench pattern centered over the contact layer and transferring the pattern by etching while employing a first etching method through the IMD layer and the second upper sub-layer of the composite etch stop layer to the first lower sub-layer of the composite etch stop layer;

etching while employing a second etch method the first lower sub-layer from the trench pattern for the interconnection lines.

2. The method of Claim 1 wherein by employing the first lower sub-layer there is avoided etching of the contact region within the first etching method.

3. The method of Claim 1 wherein the first lower sub-layer has a higher etch rate in the second etching method than the contact region;

4. The method of Claim 1 wherein forming a damascene multi-layer conductor interconnection layer is accomplished by the method further comprising:

forming a barrier metal layer over the patterned substrate; and

filling the trench pattern with a conductor material to complete the damascene multi-layer conductor interconnection layer structure.

5. The method of Claim 1 wherein the microelectronics layer is selected from the group consisting of:

microelectronics conductor layers;

microelectronics semiconductor layers;

microelectronics dielectric layers.

6. The method of Claim 1 wherein the substrate is a substrate employed within a microelectronics fabrication selected from the group consisting of:

integrated circuit microelectronics fabrications;

charge coupled device microelectronics fabrications;

solar cell microelectronics fabrications;

light-emitting diode microelectronics fabrications;

ceramic substrate microelectronics fabrications; and

flat panel display microelectronics fabrications.

7. The method of Claim 1 wherein the first lower sub-layer is formed employing a silicon oxide dielectric material formed employing plasma enhanced chemical vapor deposition (PECVD).

8. The method of Claim 1 wherein the upper second sub-layer is formed employing a silicon oxynitride dielectric material deposited employing plasma enhanced chemical vapor deposition (PECVD).

9. The method of Claim 1 wherein the contact region via conductor stud layer material is formed employing tungsten metal.

10. The method of Claim 1 wherein the inter-level metal dielectric (IMD) layer is formed employing silicon oxide dielectric material employing chemical vapor deposition (CVD).

11. The method of Claim 1 wherein the second conductor material is copper metal.

12. A method for forming a patterned microelectronics layer comprising:

providing a substrate having a contact region of tungsten metal conductor studs formed therein;

forming over the substrate a first lower organic polymer sub-layer and a second upper sub-layer to provide a composite etch stop layer;

forming over the composite etch stop layer a blanket inter-level metal dielectric (IMD) layer;

forming over the blanket IMD layer a photoresist mask layer pattern of an interconnection line trench pattern centered over the contact region and transferring the pattern while employing a first etch method through the blanket IMD layer and the second upper sub-layer of the composite etch stop layer to the first lower organic polymer sub-layer of the composite etch stop layer; and

stripping the photoresist mask pattern layer and simultaneously etching the first lower organic polymer sub-layer to complete the formation of the interconnection trench pattern centered over the tungsten metal stud contact region.

13. The method of Claim 12 wherein by employing the first lower organic polymer sub-layer there is avoided the etching of the tungsten metal stud contact region within the first etch method.

14. The method of Claim 12 wherein forming a damascene multi-layer conductor interconnection layer structure is accomplished by the method further comprising:

forming a barrier metal layer over the substrate; and

filling the interconnection trench pattern with a conductor material to complete the damascene multi-level conductor interconnection layer structure.

15. The method of Claim 12 wherein the semiconductor substrate is a silicon semiconductor substrate.

16. The method of Claim 12 wherein the first lower organic polymer sub-layer is formed employing a low dielectric constant spin-on-polymer (SOP) dielectric material.

17. The method of Claim 12 wherein the second upper sub-layer is formed employing chemical vapor deposition (CVD) of silicon containing dielectric material.

18. The method of Claim 12 wherein the inter-level metal dielectric (IMD) layer is formed of silicon oxide dielectric material employing chemical vapor deposition (CVD).

19. The method of Claim 12 wherein the conductor material employed to fill the interconnection trench is copper.

20. The method of Claim 12 wherein the barrier metal layer is formed employing tantalum nitride (TaN).